REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-31 remain pending in the application. By this Amendment, claims 1, 17 and 20-24 are amended.

In numbered paragraph 3, page 2 of the Office Action, the Examiner objects to claims 20-24 for informalities. Claims 20-24 are amended to obviate the objection. Withdrawal of the objection is respectfully requested.

In numbered paragraph 5, page 2 of the Office Action, independent claims 1 and 17, along with various dependent claims, are rejected under 35 U.S.C. §103 as being unpatentable over JP 409022380 A (Kimura) in view of U.S. Patent 6,842,800 (Dupont), JP 408272756 A (Yamagami et al.) and U.S. Patent 5,502,718 (Lane et al.). In numbered paragraph 6, page 10 of the Office Action, dependent claims 8-13 are rejected under 35 U.S.C. §103 as being unpatentable over the Kimura publication in view of the Dupont patent, the Yamagami et al. publication and the Lane et al. patent, and further in view of U.S. Patent 5,990,939 (Sand et al.). In numbered paragraph 7, page 11 of the Office Action, dependent claims 19-26 and 28-31 are rejected under 35 U.S.C. §103 as being unpatentable over the Kimura publication in view of the Dupont patent, the Yamagami et al. publication and the Lane et al. patent, and further in view of Shanley et al., PCI System Architecture, Third Edition, MindShare, Inc., 1995, pp. 39-45 and 76-89. In numbered paragraph 8, page 17 of the Office Action, dependent claim 27 is rejected under 35 U.S.C. §103 as being unpatentable over the Kimura publication in view of the Dupont patent, the Yamagami et al. publication, the Lane et al. patent and the Shanley et al. article, and

further in view of U.S. Patent 6,138,176 (McDonald et al.). These rejections are respectfully traversed.

Applicant has disclosed a method and apparatus for managing flow of information among plural processors of a processing array. The flow of data and control packet information is managed among plural processors by connecting processors within modules on a local bus, which is then connected to the system bus by way of a gateway (e.g., paragraphs [0027] and [0028]). The system bus 102 is the primary control and data path of the processor subsystem (e.g., paragraph [0027]). A system bus arbitration unit 112 of the system controller is provided for arbitrating access to the system bus by the various modules (e.g., paragraph [0026]). The system controller initiates and performs control actions. A clear path is established between various modules or devices contained on the system bus, and processors contained within modules located on local buses (e.g., paragraph [0007]).

As exemplified in Fig. 9, packet buffers are separately maintained, such as a direct memory access (DMA) packet FIFO buffer 906 and a control action (CA) FIFO buffer 914 for transmission, and DMA packet FIFO buffer 912 and a CA packet FIFO buffer 910 for reception, even though they access a common system bus. CA packet FIFO buffers (910 and 914) are maintained separate from the DMA packet FIFO buffers (906 and 912) (e.g., specification at paragraph [00136]). Accordingly, CA operations can bypass a DMA packet FIFO buffer for bus access (e.g., specification at paragraph [00152]).

The foregoing features are broadly encompassed by claim 1, which recites, among other features, an apparatus for managing flow of information among plural

processors of a processing array, including a plurality of processors, each processor being in communication with a respective local processor bus; a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus; and means for arbitrating access to at least a first portion of the system bus among said at least two processors to transfer said packets of data and control information over said first portion, said means for arbitrating establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy, and said packets being transferred using a protocol by which the system bus performs control actions for system bus access independently of said at least two processors.

On page 3 of the Office Action, the Examiner admits that the Kimura publication does not teach "said path being for packets of data and control information, control information packets being separately buffered from other packet," as recited in claim 1.

The Dupont patent does not cure the deficiencies of the Kimura publication. The Dupont patent discloses that "a buffer storage section 50 having two buffer unit sizes could be used with Internet switching hardware wherein the control packets are stored in the smaller buffer unit size buffer subsection 90 and the larger data packets are stored in the larger buffer unit size buffer subsection 100" (col. 4, lines 34-39). The motivation for the buffer subsections 90 and 100 is said to be "the small packets do not have to be stored in large buffer units that could otherwise hold a data packet, and conversely, a large data packet does not have to be segmented into a plurality

of smaller segments for storage in smaller buffer units" (col. 4, lines 39-43). However, the Dupont patent does not teach or suggest control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus. Accordingly, the Dupont patent does not teach or suggest, among other features, "a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus," as recited in claim 1.

The Yamagami et al. publication does not cure the deficiencies of the Kimura publication and the Dupont patent. The Yamagami et al. publication was applied for its disclosure of a boot process for a multiprocessor system involving arbitrated bus access according to a priority based rule. However, the Yamagami publication does not teach or suggest "a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus," as recited in claim 1.

The Lane et al. patent does not cure the deficiencies of the Kimura publication, the Dupont patent and the Yamagami et al. publication. The Lane et al. patent shows in Fig. 2 data packets exchanged through paths 26, 27 (col. 6, lines 47-60) that are separate and distinct from the command information paths 211, 214, 215. Further, the Lane et al. disclosure does not teach or suggest that these command information paths 211, 214, 215 transfer packets. At least for the

foregoing reasons, the Lane et al. patent does not cure the deficiencies of the Kimura publication, the Dupont patent, and the Yamagami et al. publication.

The Sand et al. patent, the Shanley et al. article, and the McDonald et al. patent, considered individually or in combination with the Kimura publication, the Dupont patent, the Yamagami et al. publication, and the Lane et al. patent, do not cure the deficiencies of the Kimura publication, the Dupont patent, the Yamagami et al. publication, and the Lane et al. patent. The Sand et al. patent was cited for its disclosure of a video thermal tracker interface 70 shown in Fig. 2, the Shanley et al. article was cited for its disclosure of a PCI bus operation and arbitration, and the McDonald et al. patent was cited for its disclosure of a round robin arbitration protocol (abstract; see, also, separate switched 90 and control 86 buses in Fig. 2). However, the Sand et al. patent, the Shanley et al. article, and the McDonald et al. patent, considered individually or in combination with the Kimura publication, the Dupont patent, the Yamagami et al. publication, and the Lane et al. patent, do not teach or suggest "a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus," as recited in claim 1. Claim 17 similarly recites "interconnecting at least two processors for providing a path for packets of data and control information by a system bus, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus."

For the foregoing reasons, Applicant's claims 1 and 17 are allowable. The remaining claims depend from independent claims 1 and 17, and recite additional advantageous features which further distinguish over the documents relied upon by the Examiner. As such, the present application is in condition for allowance.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully solicited.

Respectfully submitted,

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